FACULTY OF ENGINEERING
B.E. 3/4 (ECE) I – Semester (Main & Back log) Examination, December 2017
Subject: Analogy Communication

Time: 3 Hours
Max. Marks: 75

Note: Answer all Questions from Part A and any Five Questions from Part B

PART – A (25 Marks)

1. Calculate the net modulation index and power associated with AM signal $S(t) = 8 \cos 2\pi 10^6 t + 4 \cos 2\pi 10^6 t \cos 2\pi 10^4 t + 2\pi \cos 2\pi 10^5 t \cos 2\pi 10^3 t$ (3)

2. What are the properties of Hilbert transform. Find the Hilbert transform of a signal $m(t) = 2 \sin 2\pi f_m t$ (3)

3. Discuss the coherent detection of DSB-SC signals. What is Quadrature null effect? (3)

4. Compare AM and FM (3)

5. Determine the modulation index, peak frequency deviation, power and bandwidth of a single tone FM signal represented by $S(t) = 12 \cos (2\pi 10^6 t + 6 \sin 4\pi 10^2 t)$ (3)

6. When a super heterodyne receiver is tuned to 555 KHz. What is the image frequency? The antenna of this receiver is connected to the mixer via a tuned circuit whose loaded Q is 40. Find Image Frequency Rejection Ratio (IFRR) (2)

7. Define Selectivity and Sensitivity (2)

8. Where do we employ Pre-emphasis and De-emphasis circuits and Why? (2)

9. Give the classification of transmitters (2)

10. Determine the Nyquist rate of sampling for the signal $V(t) = \cos^2 6000\pi t$. What is aliasing? (2)

PART- B (10 x 5 = 50 MARKS)

11 a) Suggest a method to produce AM signal using a device having the transfer characteristic $V_o = (V_i + 2)^2$. Give the block diagram and find the amplitude sensitivity of the modulator. Draw the spectrum. (5)

b) Draw the block diagram of phase discrimination method to generate SSB-SC signal. What are the advantages of SSB-SC over other linear modulation techniques? (5)

12 a) Discuss generation of NBFM signal. Bring out the similarities and differences between NBFM and AM (5)

b) Explain the working of Foster-Seeley Discriminator for FM demodulation (5)

13 a) With a neat sketch explain the operation of Armstrong Indirect FM transmitter (6)

b) Explain different frequency tracking techniques. (4)
14 a) Derive the expression for Figure of merit (FOM) of DSB-SC system
b) Find the equivalent Noise Bandwidth of an RC low pass filter. If the Power Spectral Density of thermal noise power at the input of the filter is 2KTR, find the output noise power.

15 a) Explain the generation and detection of Pulse Position Modulated (PPM) signal with neat diagrams and waveforms
b) The front end of a television receiver having a BW of 7MHz and operating at a temperature of 27°C, consists of an amplifier having a gain of 15 followed by a mixer whose gain is 20. The amplifier has a 300Ω input resistor and a shot noise equivalent resistance of 500Ω. For the converter these values are 2.2KΩ and 13.5Ω respectively and the mixer load resistance is 470kΩ. Calculate $R_{eq}$ and RMS noise voltage for this television receiver

16 a) With necessary mathematical analysis explain Natural sampling and Flat – top sampling
b) Compare PAM, PWM and PPM

17 Write short notes on the following:
a) Choice of Intermediate Frequency
b) Vestigial Side Band Modulation

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PART – A (25 Marks)

1. Show that a RC low pass filter can work like an integrator (2)
2. Draw the response of high pass filter when the input \( f(t) = u(t) - u(t-2) \) is applied to it (3)
3. State the clamping circuit theorem (2)
4. Draw the output of the clipper given in following figure, for a sine wave input of 4v peak to peak, given \( V_{\text{ref}} = 2 \) Volts. (3)

5. Give the application of bistable multivibrator. (2)
6. What are the three types of errors that occurs in time base generators. (3)
7. Explain the concept of fan – in of a gate with an example. (3)
8. Give the design of OR gate using DTL Logic and explain its operation. (2)
9. Explain the operation of CMOS transmission gate. (2)
10. Draw the circuit of CMOS NAND gate. (3)
11 a) Derive the condition for perfect attenuation of a compensated attenuator (5)
    b) Sketch the response of a differentiator to a symmetrical square wave input of frequency 5 Khz and amplitude ± 6 Volts. Given time constant for the circuit is 5 msec.
12 a) Explain the operation of a positive peak clamper. (4)
    b) Design a clipper circuit for the following transfer characteristics assuming ideal diodes (6)
13 a) How can astable multivibrator be used as an oscillator. 
   b) Explain UTP and LTP in Schmitt trigger circuit. 

14 a) Explain working of a three input TTL NAND gate with to tempole output. 
   b) Draw the circuit diagram of a tri-state Inverter and explain its operation. 

15 a) Implement the function $F = (AB + ACD)$ using CMOS logic family. 
   b) What is significance of Totempole output in TTL logic family. 

16 a) Give the design of a sweep circuit using a UJT. 
   b) What is the advantage of open collector output and where is it used. 

17 Write short notes on: 
   a) Step response of RLC circuit 
   b) Transistor switching times 
   c) ECL logic 

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FACULTY OF ENGINEERING

BE. 3/4 (E.C.E) I – Semester (Main & Back Log) Examination, December 2017
Subject: Digital System Design with Verilog HDL

Time: 3 Hours
Max. Marks: 75

Note: Answer All Questions from part A, & Any Five Questions from part - B

PART – A (25 Marks)

1. Explain types of design methodology in verilog
2. What is the difference between $ display and $ monitor?
3. Write Verilog code for inverter in switch level modelling
4. What is meant by logic synthesis?
5. Write Verilog code for JK flip flop in behavioural modelling
6. Draw state table and diagram for mealy incompletely specified circuit
7. Explain hazards in combinational circuit with example
8. Draw ASM chart for given FSM model shown in Table 1

<table>
<thead>
<tr>
<th>RS</th>
<th>Inputs (x)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>X= 0</td>
</tr>
<tr>
<td>A</td>
<td>C,1</td>
</tr>
<tr>
<td>B</td>
<td>D,0</td>
</tr>
<tr>
<td>C</td>
<td>B,0</td>
</tr>
<tr>
<td>D</td>
<td>C,0</td>
</tr>
</tbody>
</table>

9. Explain organization of RAM
10. Draw simplified architecture of FPGA

PART- B (50 MARKS)

11 a) What are the Various Data types in Verilog HDL
   b) Write the syntax of Tri-state gates. And write a Verilog HDL code for 4-bit binary adder using 1 – bit binary adder

12 a) Explain Register Transfer Level code with example
    b) Write a Verilog HDL program in Hierarchical structural model for 3:8 decoder using 2:4 decoder and Verify with Stimulus.

13 a) Design synchronous sequential model using one hot encoding method for given state table shown in Table 1, Assume JK flip flop as storage element
14 a) Differentiate between ASM and ASMD chart
   b) Derive a Flow table that describes the behaviour of the circuit as shown

15 a) Draw and Explain operation of 6T MOSRAM cell
   b) Realize binary to gray code converter with four – input and four – output PROM

16 a) Give function $F(A, B, C, D) = m(0, 2, 7, 10) + d(12, 15)$ realize using PLA
   b) Write Verilog code using a mealy machine which detect a sequence 101 and explain with timing diagram

17 Write short notes on the following
   a) Blocking and Non blocking assignments
   b) Sequential and Parallel blocks
   c) Lookup Tables (LUTs)
FACULTY OF ENGINEERING

B.E. 3/4 (E.C.E) I – Semester (Main& Backlog) Examination, December 2017
Subject: Computer Organization and Architecture

Time: 3 Hours
Max. Marks: 75

Note: Answer all Questions from Part A and any Five Questions from Part B

PART – A (25 Marks)

1. Draw the Block Diagram of 4-bit Combinational Circuit Shifter and write its Function table. (3)
2. Write the Basic Computer instruction formats for the memory, register and I/O reference instructions. (3)
3. Differentiate between Single precision and Double precision IEEE Standard floating point representations. (2)
4. Explain briefly the microinstruction format. (2)
5. A Stack is organized in such a way that SP always points at the next empty location on the stack. List the micro – operations for the push and Pop operations. Assume stack grows downwards (3)
6. Mention the ways that computer buses can be used to communicate with memory and I/O (3)
7. Draw the flow chart for destination initiated transfer using handshaking (2)
8. What do you mean by a page fault? Which hardware is responsible for detecting the page fault? (2)
9. A non pipeline takes 50ns to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 10ns. Determine the Speed up ratio of the pipeline for 100 tasks. What is the maximum Speed up that can be achieved? (3)
10. What is meant by "locality of reference" and how does it help in faster execution of programs? (2)

PART-B (50MARKS)

11 a) Design a 4-bit Combinational Circuit decremented using four full-adder circuits (5)
   b) Draw and explain the flow chart for an interrupt cycle. Write the sequence of micro operations for the same (5)
12 a) Using Booth’s multiplication algorithm, multiply (3) x (-4) showing all the steps. (6)
   b) Compare and contrast between horizontal and vertical approach of microinstructio (4)
13 a) What is the purpose of micro program sequencer? Explain with block Diagram, how the sequencer present addresses to control memory. (5)
   b) Explain data manipulation operations of a basic computer (5)
14 a) Draw the block diagram of an asynchronous communication interface and explain its operation (5)
b) Describe in detail how data is transferred using DMA. Draw necessary diagrams to support your explanation (5)

b) What do you mean by memory hierarchy? Describe in detail (5)

16 a) Discuss SIMD processor organization (4)
b) Explain 4 possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching (6)

17 Write any TWO of the following 5 x 2 = 10
a) Stack organized instruction formats
b) Carry look ahead adder
c) Vector processing
FACULTY OF ENGINEERING
BE 3/4 (ECE) I – Semester (Main & BL) Examination, December / January 2017-18
Subject: Linear Integrated Circuits & Applications

Time: 3 Hours
Max. Marks: 75

Note: Answer All Questions From Part-A & Any Five Questions From Part-B.

PART – A (25 Marks)
1. What is a differential amplified circuit and explain why it is preferred in integrated circuits? (3M)
2. An OPAMP has a slow Rate of I V/μ sec what is the maximum frequency for which the Amplifier will given an undistorted sinusoidal output signal if applied input signal is 10Vp-p. (2M)
3. What is meant by virtual ground? Explain. (2M)
4. Draw the OPAMP Subtractor circuit and derive the expression for output voltage. (2M)
5. What are the advantages of higher order fitters over first order fitters. (3M)
6. Explain the operation of clippers using precision rectifiers. (3M)
7. Define lock range & capture range of PLL. (2M)
8. What are the specifications of Digital to analog converters. (3M)
9. Explain the features of fixed voltage regulators. (2M)
10. Define the terms resolution and conversion time of A/D converters. (3M)

PART – B (50 Marks)
11. a) Define the following OPAMP electrical parameters (i) input bias current (ii) input offset current (iii) input offset Voltage and (iv) output Offset Voltage. Also write the expression for output offset due to above parameters (5M)

b) For a given differential amplifier, two sets of input signals are applied. First Set is (i) \( V_{S1} = V_{S2} = 50\text{mV} \), Second Set is (ii) \( V_{S1} = 100\mu V \), \( V_{S2} = 140\mu V \). If differential gain is 2000 and CMRR=100dB find output due to both sets Of input signals. (5M)

12. a) Explain the operation of instrumentation amplifier using the OPAMPS with neat diagram and relevant expressions. (6M)

b) Design a practical differentiator which operates upto a frequency of 1.5 KHZ. (4M)

13. a) Draw and explain the operation of second order low pass active filter and derive the expression for its cut off frequency (6M)

b) Explain the operation of schmitt trigger using OP AMP. (4M)

14. a) Draw a circuit diagram of Triangular wave generator using OP - AMP and derive expression for its frequency of oscillation? (7M)
-2-

b) Explain the concept of $P_{LL}$ with block diagram

15 a) Explain the operation of IC 723 as low Voltage Regulator

b) Explain the operation of successive approximation type ADC with an example

16 a) Draw the functional diagram of XR 2206 function generator and explain its Operation.

b) Explain the operation of sample and hold circuit using OPAMP.

17 Write Short notes on

a) Voltage controlled oscillators

b) Flash type ADC.
FACULTY OF ENGINEERING
B.E. 3/4(ECE) I- Semester(Main & Backlog) Examination, Dec, 2017
Subject: Automatic Control Systems

Time: 3 hours
Max. Marks: 75

Note: Answer all questions from Part-A and any Five Questions from part-B

PART - A (25 Marks)

1. Distinguish between open loop and closed loop control system?
2. "Potentiometer acts as a error detector" Justify.
3. The standard form of a second order system whose closed loop poles are located at \( S = -3 \pm j4 \) then calculate rise time.
4. The transfer function of forward path and feed back element is given by
   \[ G(S) = \frac{S + 4}{S(S + 2)}, \quad H(S) = \frac{S^2 + 2S + 3}{S(S^2 + 5S + 4)} \]
   then determine type and order of the system.
5. Define gain margin and phase margin.
6. What is principle of argument?
7. List out the drawbacks of digital control system?
8. Compare analog and digital control system.
9. Compute resolvent matrix if the system matrix \( A = \begin{bmatrix} 1 & 2 \\ 3 & 4 \end{bmatrix} \).
10. Write the properties of state transition matrix.

PART - B (50 Marks)

11. Determine transfer function \( \frac{C(S)}{R(S)} \) for a given system using block diagram reduction technique.
12. The open loop transfer function of a control system is 
\[ \frac{K}{S(S+2)(S^2+2S+5)} \] 

i) Draw the root locus and determine closed loop system stability. [7]

ii) Determine the value of \( K \) at any break away point. [3]

13. a) Determine the range of \( K \) such that the characteristic equation 
\[ S^3 + 3(K + 1)S^2 + (7K + 5)S + 4K + 7 = 0 \] has roots more negative than -1 [4]

b) A unity feedback system is characterized by an open loop transfer function
\[ G(S) = \frac{K}{S(S+5)} \]. Determine the gain 'K' so that the system will have damping ratio of 0.4. For the value of 'K' determine setting time, peak over shoot and peak time. [6]

14. The open loop transfer function of a system is given by
\[ G(S) = \frac{K(S+2)}{S^2(S+4)} \]. Sketch the nyquist plot and determine range of \( K \) for closed loop system to be stable. [10]

15. a) Describe the architecture of a digital control system. [4]

b) Obtain the unit step response of the system shown in figure if
\[ G(S) = \frac{1}{S(S+2)} \]. [6]

16. A system is characterized by the following state equations.
\[
\begin{bmatrix}
\dot{x}_1 \\
\dot{x}_2
\end{bmatrix} = \begin{bmatrix}
-3 & 2 \\
-4 & 0
\end{bmatrix} \begin{bmatrix}
x_1 \\
x_2
\end{bmatrix} + \begin{bmatrix}
0 \\
1
\end{bmatrix} u \quad y = \begin{bmatrix}
1 & 0
\end{bmatrix} \begin{bmatrix}
x_1 \\
x_2
\end{bmatrix}
\]

i) Find the transfer function of the system. [5]

ii) Identify whether the given system is controllable or not. [5]

17. Write short notes on the following
i) Lag and Lead Compensators.
ii) Synco's
iii) Gain Margin and Phase Margin