FACULTY OF ENGINEERING

Subject : Linear Integrated Circuits and Applications

Time : 3 Hours
Max. Marks: 75

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1. Define slew rate. Explain its significance and give its typical value for 741 IC. (2)
2. Define input bias current, input offset voltage and write the expression for output voltage of OP AMP due to these parameters. (3)
3. What are the desirable characteristics of Instrumentation Amplifier? (3)
4. Explain OP AMP subtractor circuit and derive the expression for its output voltage. (3)
5. What are the advantages of higher order filters over first order filters? (2)
6. Explain the operation of Astable multivibrator using OP AMP. (3)
7. Define Lock range and capture range of PLL. (2)
8. Draw the functional diagram of NE 555 and represent all pins. (2)
9. What do you understand by current fold back in IC 723 Regulators? (3)
10. Define the terms Resolution and conversion time of A/D converters. (2)

PART – B (50 Marks)

11. (a) Obtain the expressions for differential voltage gain, common mode gain, input impedance and output impedance of dual input unbalanced output differential amplifier. (8)
   (b) What is the need for frequency compensation in an OP AMP? Explain about any one frequency compensation technique. (4)

12. (a) Design a practical differentiator which operates between 150 Hz to 1500 Hz. (5)
    (b) Explain the operation of sample and hold circuit with neat diagram and waveforms. (5)

13. (a) Draw the circuit diagram of narrow band pass filter and derive the expressions for its voltage gain, band width and quality factor. (6)
    (b) Explain the operation of peak detector circuit. (4)

14. (a) Draw the circuit diagram of monostable multivibrator using 555 timer and explain its operation. Also derive the expression for pulse width. (6)
    (b) Explain the operation of Schmitt Trigger using OP AMP. (4)

15. (a) Explain the operation of IC 723 as high voltage Regulator. (4)
    (b) Explain the operation of successive approximation ADC with an example. (6)

16. (a) Explain the operation of practical logarithmic Amplifier. (5)
    (b) What are the different ways to improve CMRR of OP AMP? Explain any one method. (5)

17. Write short notes on the following:
    (a) All pass filters (5)
    (b) Voltage controlled oscillators (5)

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PART - A (25 Marks)

1. Explain the need for attenuation.
2. State clamping circuit theorem.
3. Difference between astable and Bistable multivibrator.
4. List the features of time base signal.
5. Define Figure of merit.
6. List the integrated circuit package type.
7. Explain Fan-in and Fan-out in CMOS.
8. Explain how a LPF acts as an Integrator.
9. List the application of clipper and clamper.
10. Compare CMOS and TTL.

PART - B (50 Marks)

11. (a) Sketch the output response for following clipper circuit when input is linearly varying from 0 to 150V. Assume diodes are ideal.

```
   +------------------+
   |                  |
   |        D1        |
   +------------------+
   |                  |
   |                  |
   |                  |
   +------------------+
   |                  |
   |        100k      |
   +------------------+
   |                  |
   |                  |
   |                  |
   +------------------+
   |                  |
   |        200k      |
   +------------------+
   |                  |
   |                  |
   +------------------+
   |                  |
   |        2xV      |
   +------------------+
   |                  |
   |                  |
   +------------------+
   |                  |
   |        100V      |
   +------------------+
   |                  |
   |                  |
   +------------------+
   |                  |
   |                  |
   +------------------+
   |
   +------------------+
   |                  |
   |        D2        |
   +------------------+
   |                  |
   |                  |
   +------------------+
   |                  |
   |                  |
   +------------------+
   |                  |
   +------------------+
   |

(b) Explain positive clamper.

12. (a) Define the three types of error that occur in time base generator.
   (b) Draw the circuit of monostable multivibrator and derive the expression for pulse width.

13. (a) Compare differentiator and integrator.
   (b) Explain the response of a low pass RC circuit for square wave input.

14. (a) Design and analyze sweep circuit using UJT.
   (b) Derive Intrinsic = standoff ratio.

15. Draw and explain three input ECL OR / NOR Gate.

16. Why totempole is used in DTL draw the circuit diagram and explain a DTL gate?

17. Write short notes on any two of the following:
   (a) Attenuator
   (b) Schmitt Trigger
   (c) IC characteristics

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FACULTY OF ENGINEERING


Subject : Analog Communication

Time : 3 Hours

Max. Marks: 75

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1. Define the term modulation index for AM.

2. Write the methods of generation for SSB-SC signal.

3. Derive an expression for single tone FM wave.

4. In an FM system if modulation index is doubled and modulating frequency is reduced four times, what is the effect on the frequency deviation?

5. Write the advantage of super heterodyning.

6. Explain the operation of a noise limiter in FM receivers?

7. State central limiting theorem.

8. Explain noise equivalent bandwidth.

9. Explain in brief about Bit interleaving in TDM.

10. What is need of Pulse modulation?

PART – B (50 Marks)

11. (a) Explain the operation of a balanced slope detector, giving circuit diagram and response characteristic. What are its draw backs?

(b) Derive an expression for the total transmitter power in the AM wave. Also obtain its efficiency.

12. (a) Explain the Armstrong method of FM generation.

(b) An FM wave is represented by \( V = 12 \sin (6 \times 10^8 t + 5 \sin 1250 t) \). Find the carrier and modulating frequencies, the modulation index and maximum deviation of FM wave. Is it narrow band or wideband FM? What power this FM will dissipate in a 10 ohm resistor?

13. (a) Draw the block diagram of Super heterodyne receiver designed to receive FM signals and explain its working.

(b) Explain about choice of intermediate frequency in AM receiver.

14. (a) Find the power spectral density of Noise in case of SSB-SC and also calculate Figure of merit.

(b) Calculate the system noise of a receiver that has a bandwidth of 6 MHz and an input noise temperature of 25°K to the antenna. The equivalent noise resistance of receiver is 75 ohms. The antenna has a resistance of 72 ohms. Assume \( T_o=290^\circ K \).
FACULTY OF ENGINEERING

Subject: Automatic Control Systems

Max. Marks: 75

Time : 3 Hours

Note: Answer all questions from Part-A and answer any five questions from Part-B. Missing data, if any, may suitably be assumed.

PART – A (25 Marks)

1. Discuss about the block diagram and its components of a Control system.
2. What are the properties of Signal flow graphs?
3. Give the steady state error values to standard inputs for Type 2 system.
4. Describe the transient and steady state response of a Control system.
5. Analyze the effects of addition of open loop poles.
6. Illustrate the need for a Compensator? Derive the transfer function of a lead compensator network and draw its characteristics.
7. With the help of detailed block diagram explain Digital control system with signal convertors.
8. Draw the circuit of sample and hold circuit and obtain its transfer function.
9. Mention the need for State variables.
10. Find the State transition matrix for

\[
A = \begin{bmatrix}
0 & -1 \\
+2 & -3
\end{bmatrix}
\]

PART – B (50 Marks)

11 (a) Negative feedback is preferred in Control Systems. Justify.
(b) Write the differential equations governing the mechanical system shown in figure. Also draw the force-voltage and force-current analogous circuit.

12 (a) A unit ramp input is applied to a unity feedback system whose output response is 
\[ C(s) = \frac{100}{s^2 + 5s + 100} \]. Analyze the time response and steady state error.
(b) Explain the rules to construct a root locus.

13 For the system with transfer function, draw the Bode Plot and obtain Gain margin and Phase margin.

\[ G(s) = \frac{400(s + 2)}{s^2(s + 5)(s + 10)} \]
14. (a) For the system shown in fig., find the response at sampling instants to unit step input for \( T = 1 \) Sec and \( K = 1 \).

(b) Obtain the expression for \( C(z) \) in terms of \( R(z) \) of a basic closed loop discrete control system.

15. (a) What are the advantages of State space representation?
(b) A system is described by the following differential equations. Obtain State space representation of the system.

\[
\begin{align*}
\frac{d^2 x}{dt^2} + 3 \frac{dx}{dt} + 4x &= u_1(t) + 3u_2(t) + 4u_3(t) \\
y_1 &= 4 \frac{dx}{dt} = 3u_1, \quad y_2 = \frac{d^2 x}{dt^2} + 4u_2 + u_3
\end{align*}
\]

16. (a) Illustrate any two limitations of Routh stability criterion.
(b) Determine State Controllability and Observability of the system described by

\[
\begin{bmatrix}
x'_1 \\ x'_2 \\ x'_3
\end{bmatrix} =
\begin{bmatrix}
0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & -2 & -3
\end{bmatrix}
\begin{bmatrix}
x_1 \\ x_2 \\ x_3
\end{bmatrix} +
\begin{bmatrix}
0 \\ 0 \\ 10
\end{bmatrix} u,

y = [1 \ 0 \ 0]
\begin{bmatrix}
x_1 \\ x_2 \\ x_3
\end{bmatrix}
\]

17. Write Short notes on:
(a) Translational system Vs Rotational system
(b) BIBO Stability
(c) PID Controller

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PART - A (25 Marks)

1. Differentiate between force-voltage and force-current analogy for mechanical (translational and rotational) and electrical systems. [2]
2. Define Mason’s gain formula and discuss the advantages over block diagram reduction techniques. [3]
3. Define steady state error and write the expression for it. [2]
4. Define and order and type of a system with an example. [3]
5. What is principle of argument? [2]
6. Derive the transfer function of Lag-lead compensator network and draw its characteristics. [3]
7. With the help of detailed block diagram explain Digital control system with signal convertors. [2]
8. Compare Analog and Digital control systems. [3]
9. Discuss the significance of state space analysis. [2]
10. Define Controllability and Observability. [3]

PART - B (50 Marks)

11. (a) Classify various types of control systems and give examples for open loop and closed loop control systems. [4]
    (b) Write the differential equations governing the mechanical system shown in figure. Also draw the force-voltage and force-current analogous circuit. [6]

12. Sketch the root locus of the system whose open loop transfer function is
    \[ G(s) = \frac{K}{s(s + 2)(s + 4)} \]. Find the value of K so that the damping ratio of the closed loop system is 0.5. [10]

13. (a) Mention various advantages for investigating the system performance in frequency domain than time domain. [5]
    (b) Sketch the Bode Plot and find out the stability for \[ G(s) = \frac{10}{s(s + 10)} \]. [5]
14. (a) Obtain the expression for $C(z)$ in terms of $R(z)$ of a basic closed loop discrete control system. [4]
   (b) For a system having $G(s) = \frac{1}{s+2}$ and $H(s) = 1$, find the output value at sampling instants for unit step input $r(t)$. Take sampling interval $T = 0.5$ sec. [6]

15. (a) Write the properties of State transition matrix. [6]
   (b) Find the solution of the state equation to an unit step input. [4]

16. (a) Sketch Bode plot for the following transfer function and determine the system gain $K$ for the gain cross over frequency to be 5 rad/sec.

$$G(s) = \frac{Ks^2}{(1+0.2s)(1+0.02s)}.$$ [6]

   (b) Classify various types of Compensators and explain briefly. [4]

17. Write Short notes on:
   (a) Error sensing devices
   (b) Digital control systems using state space
   (c) Modern control theory vs Conventional control theory [10]
FACULTY OF ENGINEERING


Subject: Computer Organization and Architecture (New)

Time: 3 Hours Max.Marks: 75

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1. Represent a condition evaluation of a typical expression using RTL with two examples. [2]
2. Specify a sequence of micro-operations that will perform the operation:
   a) \( IR \leftarrow M[PC] \)
   b) \( AC \leftarrow AC + TR \)
   c) \( DR \leftarrow DR + AC \) [3]
3. Show the hardware for implementing Booth's algorithm. [3]
4. Why do we use dividend alignment while performing division operation of binary numbers? [2]
5. Compare Hardwired and Micro programmed control unit. [2]
6. Write the differences between 2 and 3 address instructions. [2]
7. Why does DMA have priority over the CPU when both request a memory a memory transfer? [2]
8. Explain the terms Tag, Index and Block in relation to cache memory. [3]
9. How many \( 128 \times 8 \) RAM chips are needed to provide a memory capacity of \( 2048 \times 16 \) words? [2]
10. Distinguish between Superscalar and VLIW processors. [3]

PART – B [50 Marks]

    b) List the control functions and micro-operations needed for the execution of the following instructions and explain.
       i) ADD [5]
       ii) BSA

12. a) Explain the process of floating point number multiplication with flow chart. [5]
    b) Show the hardware for a 2 bit-by-2 bit array multiplier and explain its working. [5]

13. a) Write the need for addressing modes. Explain various addressing mode supported by a general purpose CPU. [6]
    b) Show how a 9-bit micro-operation field in a microinstruction can be divided into subfields to specify 46 micro-operations. How many micro-operations can be specified in one microinstruction? [4]

14. a) Design a parallel priority interrupt hardware for a system with four interrupt sources. [5]
    b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is \( 128 \times 32 \).
       i) Formulate all pertinent information required to construct the cache memory [5]
       ii) What is the size of the cache memory?
b) List and briefly describe types of Superscalar instruction issue policies. [5]

16 a) Differentiate between Restoring and Non-Restoring division algorithms. [4]
b) Explain instruction pipeline conflicts and their remedies. [6]

17 Write any Two of the following [5 x 2 = 10]
   a) Isolated Vs Memory mapped I/O.
   b) Common bus system.
   c) Instruction level parallelism

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FACULTY OF ENGINEERING
Subject: Digital System Design with Verilog HDL

Time: 3 Hours
Max. Marks: 75

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1. Explain System tasks and Compiler directives in Verilog. (2)
2. Explain representation of numbers in Verilog. (2)
3. Write a Verilog module to describe 2 bit comparator in data flow modeling. (3)
4. What is RTL code with example? (2)
5. Explain difference between mealy and moore model. (3)
6. Define ASM blocks and explain with example. (3)
7. Write a Verilog model for JK Flip Flop. (2)
8. Explain analyze procedure of asynchronous sequential circuits. (2)
9. Explain Race conditions with example. (3)
10. Draw simplified architecture of FPGA and CPLD with applications. (3)

PART – B (50 Marks)

11. (a) Explain generated block with example.
   (b) Write Verilog behavioural model to model 8 bit ALU with 8 instructions with test bench. Draw input and output waveforms.

12. Design and write Verilog code for modulo 8 counter using sequential approach use T flip flop as memory element.

13. (a) Differentiate between latch and Flip flop.
   (b) Design sequential circuit for given state table and write Verilog code in behavioural modeling.

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<th>A</th>
<th>B/O</th>
<th>C/I</th>
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<td>E/O</td>
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<tr>
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<td>A/I</td>
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14. Analyze the given Synchronous sequential Circuit and write its Verilog code.

15. Design Vending machine controller and Implement its Verilog code.

16. Analyze given asynchronous sequential circuit and obtain its state table and timing diagram.

17. Write short notes on the following:
   (a) Multway Branching
   (b) Programmable Logic Devices (PLDs)
   (c) Memory Devices

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