Code No. 9241

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I-Semester (Main) Examination, December/January 2014-15

Subject : VLSI Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1 Implement the logic function of $f = \overline{ab + \overline{C}}$ using CMOS logic. (3)
2 Draw 2-to-1 MUX using Transmission gate logic. (3)
3 How latch up problems in CMOS logic is eliminated? (3)
4 Draw the Layout of a CMOS inverter. (3)
5 How the delay is reduced in an invertor cascade mode? (2)
6 Explain the Read operation of Dynamic RAM cell. (2)
7 What is the effect of charge storage on floading gate? (2)
8 Define rise time, fall time and propagation delay. (3)
9 What are modeling styles are there in verilog HDL? (2)
10 What is meant by floor planning? Give its structure. (2)

PART – B (50 Marks)

11 (a) Derive current equation of an nMOS transistor in saturation region. (5)
(b) Implement the logic function $f = \overline{a.(b + c)}$ using CMOS logic and explain with the help of its truth table. (5)

12 (a) What are the different types of layers that are present in a MOSFET? (5)
(b) How to obtain series and parallel transistor structures in complex logic circuits? (5)

13 (a) What is Lambda? Explain the lambda based design rules. (5)
(b) What is a standard cell? Draw cell concepts in cell based design. What is a primitive cell? (5)

14 (a) Explain the different steps involved in fabrication of VLSI chip. (5)
(b) Derive the expressions for rise time and fall time. (5)

15 (a) Draw 6T sRAM cell. Explain its read and write operation. (5)
(b) Implement XOR-XNOR logic gate using differential cascode voltage switch logic. (5)

16 (a) Derive expression for the delay of a multiple rung ladder circuit. (5)
(b) Develop a verilog behavioural model of full ladder. (5)

17 Write a short notes on :
(a) High speed adder (3)
(b) RC switch model equivalent for NAND gate (3)
(c) Inter connect modeling (4)

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