FACULTY OF ENGINEERING
B.E. 4/4 (IT) I – Semester (Suppl.) Examination, June / July 2015
Subject: VLSI Design

Time: 3 Hours
Max. Marks: 75

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A

1 Why silicon technology is more preferred in CMOS technology? (2)
2 What are the different capacitances present in MOS transistor. (2)
3 Draw layout of two input NOR gate. (3)
4 How to obtain n+ and p+ regions. (2)
5 Draw RC equivalent circuit of a CMOS NAND gate. (3)
6 How to measure the propagation delay of CMOS inverter? Define rise time, fall time and delay time. (3)
7 What are the advantages of pseudo-nMOS over CMOS technology? (2)
8 Distinguish between DRAM and SRAM. (3)
9 Write a venlog data flow model of full adder. (3)
10 What is meant by interconnect? Give its physical model. (2)

PART – B

11 a) Derive the nMOS transistor current equation in resistive region. (5)
    b) Design 4x1 MUX using transmission logic gate. Give its truth table. (5)
12 a) With help of neat structure, how to make the transistors in series and parallel connections. (5)
    b) Difference between active contact and poly contact. Draw stick diagram of the function f = \overline{A}+BC. (5)
13 a) Draw and explain CMOS process flow. (5)
    b) With a neat sketch, explain the CMOS inverter switching characteristics. (5)
14 a) Explain charge leakage and charge sharing mechanism in dynamic CMOS logic. (5)
    b) Implement Two input XOR / XNOR logic using differential pass transistor logic. (5)
15 a) Draw and explain VLSI design flow. (5)
    b) Implement 4x4 array multiplier? Give one example. (5)
16 a) Write a behavioural model of 4-bit comparator using venlog. (5)
    b) What is cross talk? How it is modeled in MOS technology. (5)
17 Write short notes on:
   a) Latch up and its prevention (4)
   b) ROM and PLA (3)
   c) Barrel shifter (3)

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