

FACULTY OF INFORMATICS

B.E. 2/4 (IT) I - Semester (Supplementary) Examination, June / July 2015

Subject : Digital Electronics and Logic Design

Time : 3 hours

Max. Marks : 75

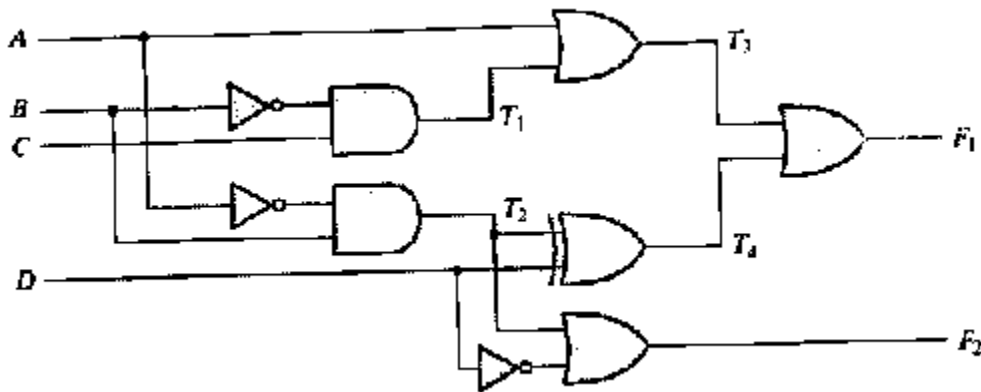
Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

- | | |
|---|---|
| 1 Using algebraic manipulation prove that $(x + y)(x + y') = x$. | 2 |
| 2 Implement XOR and XNOR gate using NAND gates only. | 2 |
| 3 Write the advantages of designing custom chips. | 2 |
| 4 State and prove DeMorgans law. | 3 |
| 5 What is the difference between a latch and a Flipflop. | 3 |
| 6 Write VHDL code for a Half Adder circuit. | 3 |
| 7 Define Minterm and Maxterm. | 3 |
| 8 Draw the timing diagram of Master slave D Dlipflop. | 2 |
| 9 What are the advantages of custom chips? | 3 |
| 10 Define Fan-in and Fan-out. | 2 |

PART – B (50 Marks)

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|--|---|
| 11 Consider the combinational circuit shown in the figure. | 7 |
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|--|-----|
| a) Derive the Boolean expressions for T_1 through T_4 . Evaluate the outputs F_1 and F_2 as a function of the four inputs. List out the truth table for 16 binary combinations along with the values for T_1 through T_4 and outputs F_1 and F_2 in the table. | 3 |
| b) Write the VHDL code for the above given combinational circuit. | 6 |
| 12 a) Prove the following equations using the Boolean algebraic theorems : | 6 |
| i) $A + A'.B + A.B' = A + B$ | |
| ii) $A'BC + A B' C + ABC' + ABC = AB + BC + AC$ | |
| b) Implement the following Boolean function using NAND gates : | 4 |
| $F(x, y, z) = (1, 2, 3, 4, 5, 7)$ | ..2 |

- 13 a) Explain with a neat diagram carry look ahead adder. 6
b) Design and implement a full adder using decoder. 4
- 14 a) Show how a JK Flipflop can be constructed using a D Flipflop and other logic gates. And explain its working. 7
b) Write the characteristic table of JK flipflop and D Flipflop. 3
- 15 a) Explain FSM as an Arbiter circuit. 7
b) Differentiate synchronous and asynchronous sequential circuits. 3
- 16 a) Draw the internal architecture of FPGA and explain. 5
b) Design and implement a right shift register. 5
- 17 Write short notes on :
a) Clock skew 3
b) Path Sensitizing 4
c) Stuck-at Model 3
