PART – A (25 Marks)

1. Using algebraic manipulation prove that \((x + y)(x + y') = x\).
2. Implement XOR and XNOR gate using NAND gates only.
3. Write the advantages of designing custom chips.
4. State and prove DeMorgans law.
5. What is the difference between a latch and a Flipflop.
6. Write VHDL code for a Half Adder circuit.
7. Define Minterm and Maxterm.
8. Draw the timing diagram of Master slave D Flipflop.
9. What are the advantages of custom chips?

PART – B (50 Marks)

11. Consider the combinational circuit shown in the figure.

   a) Derive the Boolean expressions for \(T_1\) through \(T_4\). Evaluate the outputs \(F_1\) and \(F_2\) as a function of the four inputs. List out the truth table for 16 binary combinations along with the values for \(T_1\) through \(T_4\) and outputs \(F_1\) and \(F_2\) in the table.

   b) Write the VHDL code for the above given combinational circuit.

12. a) Prove the following equations using the Boolean algebraic theorems:
   i) \(A + A' \cdot B + A \cdot B' = A + B\)
   ii) \(A'BC + A \cdot B' \cdot C + ABC' + ABC = AB + BC + AC\)

   b) Implement the following Boolean function using NAND gates:
   \(F(x, y, z) = (1, 2, 3, 4, 5, 7)\)
13 a) Explain with a neat diagram carry look ahead adder.  
   b) Design and implement a full adder using decoder.

14 a) Show how a JK Flipflop can be constructed using a D Flipflop and other logic gates. And explain its working.  
   b) Write the characteristic table of JK flipflop and D Flipflop.

15 a) Explain FSM as an Arbiter circuit.  
   b) Differentiate synchronous and asynchronous sequential circuits.

16 a) Draw the internal architecture of FPGA and explain.  
   b) Design and implement a right shift register.

17 Write short notes on:  
   a) Clock skew  
   b) Path Sensitizing  
   c) Stuck-at Model