



Code No. : 6224/O/S

**FACULTY OF INFORMATICS**  
**B.E. 4/4 (IT) I Semester (Old) Examination, July 2014**  
**VLSI DESIGN**

Time : 3 Hours]

[Max. Marks : 75

**Note :** Answer **all** questions from Part – A. Answer **any five** questions from Part – B.

**PART – A**

**(25 Marks)**

1. What is Moore's law ? 2
2. Explain the operation of transmission gate logic ? Give its truth table. 2
3. Draw the physical structure of a nMOSFET and indicate all the layers. 2
4. What is latch up ? How do you prevent latch up problem in CMOS logic ? 3
5. What is lambda ? Give some ( $\lambda$ ) based design rules ? 2
6. Define rise time, fall time and delay time. 3
7. Draw Pseudo nMOS logic block diagram. What are the advantages and disadvantages of this logic. 2
8. Explain about NOR based ROM cell. 3
9. Write verilog model for the half adder. 3
10. Draw full adder using half adder only. 3

**PART – B**

**(5×10=50 Marks)**

11. a) Design a NAND<sub>3</sub> gate using an 8 × 1 mux. 5  
b) Construct the CMOS logic gate for the function  $F = \overline{x(y+z)} + y$ . 5
12. a) An interconnect line is made from a material that has a resistivity of  $\rho = 4 \mu\Omega\text{-cm}$ . The interconnect is 1200 Å thick. The line has a width of 0.6  $\mu\text{m}$ .
  - i) Calculate the sheet resistance  $R_s$  of the line.
  - ii) Find the line resistance for a line of 125  $\mu\text{m}$  long. 5  
b) Draw the layout of two input NAND gate also draw the stick diagram. 5
13. Explain the CMOS process flow diagrams. 10
14. a) Draw and explain the CMOS inverter DC characteristics. 5  
b) Explain dynamic CMOS logic circuit and what is precharge and evaluation charge sharing. 5
15. a) Explain the operation of SRAM cell and DRAM cell. 5  
b) Compare SRAM with DRAM. 5
16. a) Discuss about multiple Rung ladder circuit. How to model the RC interconnect to measure the delay. 5  
b) Explain about carry look ahead adder and multipliers with help of an example and circuit setup. 5
17. a) What is meant by floor planning and routing explain ? 5  
b) Implement 8 × 1 mux using 2 × 1 mux use TG logic. 5