BIT-401

VLSI DESIGN

UNIT-I

An overview of VLSI, Moore's law, Electrical Conduction in Silicon, Electrical Characteristics of MOSFETs Threshold voltage, nFET Current-Voltage equations, square law and linear model of a FET, MOS capacitances, gate- source and gate drain capacitances, junction capacitances in a MOSFET, RC model of a FET, modeling small MOSFET, scaling. MOSFET as switches, pass characteristics, logic gates using CMOS, Bubble pushing, XOR and XNOR gates, AOI and OAI logic gates, transmission gates. TG based 2-to-1 MUX, XOR, XNOR, OR circuits.

UNIT-II

Physical structure of CMOS ICs, IC layers, layers used to create a MOSFET, Top and side view of MOSFETs, Silicon patterning or layouts for series and parallel connected FETs. Layouts of NOT gate, transmission gate, noninverting buffer, NAND2, NOR2, Complex logic gate, 4 input AOI gate. Stick diagram representations. Layouts of Basic Structure: nwells, active area definition, design of n^+, p^+ regions, masks for the nFET, active contact cross section and mask set, metal1 line with active contact, poly contact: cross section and layout, vias and higher level metals. Latchup prevention.

UNIT-III

Fabrication of CMOS ICs, CMOS process flow, Design rules: minimum space width, minimum spacing, surround, extension, cell concepts and cell based design, logic gates as basic cells, creation of new cell using basic gates. DC characteristics of the CMOS inverter symmetrical inverter, layouts, Inverter switching characteristics, RC switch model equivalent for the CMOS inverter, fanout, input capacitance and load effects, rise time and fall time calculation, propagation delay, driving large capacitive loads, delay minimization in an inverter cascade.

UNIT-IV

Pseudo nMOS, tristate inverter circuits, chocked CMOS, charge leakage, Dynamic CMOS logic circuits, precharge and evaluation charge sharing, Domino logic, Dual rail logic networks, differential Cascade Voltage Switch Logic (CVSL) AND/NAND, OR/NOR gates, Complementary Pass Transister Logic (CPL). The SRAM, 6T SRAM cell design parameters, writing to an SRAM, resistor model, SRAM cell layout, multi port SRAM, SRAM arrays, Dynamic RAMs: 1T RAM cell, charge leakage and refresh in a DRAM cell, physical design of DRAM cells. NOR based ROM, ROM array using pseudo nMOS circuitry, floating gate MOSFET, effect of charge storage on the floating gate, A E^2PROM word using floating gate nFETs, logic gate diagram of the PLA, NOR based design, CMOS PLA, Gate arrays.

UNIT-V

VLSI Design flow, structural gate level modeling, gate primitives, gate delays, switch level modeling, behavioral and RTL operators, timing controls, blocking and non blocking assignments, conditional statements, Data flow modeling and RTL, Comparator and priority encoder barrel shifter, D latch Master slave D type flip-flop, Arithmetic circuits; half adder, full adder, AOI based, TG based, ripple carry adders, carry look ahead adders, High speed adders, multipliers. Interconnect modeling; Interconnect resistance and capacitance sheet resistance Rs, time delay, single and multiple rung ladder circuits, simple RC inter connect model, modeling inter connect lines with a series pass FET, cross talk, floor planning and routing, clocking, Testing of VLSI circuits.

Suggested Reading:

1) John P. Uyemura, "Introduction to VLSI circuits and Systems", John Wiley & Sons, 2002
2) John P. Uyemura, "Chip design for submicron VLSI: CMOS layout and simulation" IE, Cengage learning, 2006.
3) Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design" 3rd Edition, PHI, 2000.
4) Jan M. Rabey and others "Digital Integrated Circuits A design perspective", Pearson Education