BIT431

VLSI DESIGN LAB

1. Switch level modeling using Verilog
   a) Logic gates
   b) b) AOI and OAI gates
   c) c) Transmission gate
   d) Complex logic gates using CMOS

2. Structural Gate-level Modeling [With and Without delays] – Digital circuits using gate primitives – using Verilog.
   a) AOI gate
   b) b) Half adder and full adders
   c) c) MVX using buffers
   d) S-R latch etc.

3. Mixed gate –level and Switch-level modeling using Verilog-usage of primitives, modules and instancing and understanding the hierarchical design.

   a) Constructing a 4-input AND gate using CMOS 2-input NAND and NOR gates.
   b) constructing a decoder using CMOS 2-input AND gates and NOT gates etc.

4. RTL Modeling of general VLSI system components.
   a) MUXes
   b) b) Decoders
   c) Priority encodes
   d) Flip-flops
   e) Registers.

5. Synthesis of Digital Circuits
   a) Ripple carry adder and carry look-ahead adder
   b) array multiplier

6. Verilog code for finite state machine

7. Modeling of MOSFET

8. Stick diagram representations. Simple layouts of Inverter. Understanding the concepts of Design Rule checking.

9. Fault Modeling for Stuck-at-O and Stuck-at-1 faults.

10. Clock generation circuit(study)