Code No. 2032

FACULTY OF INFORMATICS

B.E. 2/4 (IT) I – Semester (Suppl.) Examination, June 2013

Subject: Digital Electronics and Logic Design

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1. Differentiate between standard chips and custom-designed chips. (3)
2. Give the logic network that implements $f = \bar{x}_1 + x_1.x_2$ (2)
3. State Shannon's Expansion Theorem. (2)
4. Implement 4:1 multiplexer using 2:1 multiplexers. (3)
5. Compare and contrast Latch and flip-flop. (2)
6. Define set up time and hold time of a latch. (3)
7. Distinguish between combinational circuits and sequential circuits. (2)
8. Write the significance of hazards. (2)
9. State the conditions for compatibility of states. (3)
10. Write short notes on digital System. (3)

PART – B (50 Marks)

11.(a) Using algebraic manipulation show that $\sum M(1,2,3,4,5,6,7) = x_1 + x_2 + x_3$. (5)

(b) Realize the switching function after simplification $f(x_1, x_2, x_3) = \pi M(0, 1, 5, 7)$. (5)

12.(a) Explain the general structure of a PLA. (5)

(b) Realize the functions $f_1 = x_1x_2 + x_1\bar{x}_3 + \bar{x}_1\bar{x}_2x_3$

$f_2 = x_1x_2 + \bar{x}_1\bar{x}_2x_3 + x_1x_3$ using PLA. (5)

13.(a) find the minimum-cost SOP and POS forms for the function

$f(x_1, x_2, x_3, x_4) = \pi M (0, 1, 2, 4, 5, 7, 8, 9, 10, 12, 14, 15)$. (5)

(b) Design 4:1 multiplexer using a decoder. (5)

14.(a) With a neat diagram explain Master-slave D flip-flop with clear and preset. (5)

(b) Design a modulo-6 counter with synchronous reset. (5)

15. Illustrate state-assignment problem using sequential circuit approach. (10)
16. With an example explain the behaviour of asynchronous sequential circuit. (10)
17. Write short notes on:
    (a) State reduction (4)
    (b) PLDs (3)
    (c) ASM charts (3)

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Code No. 2039

FACULTY OF ENGINEERING

B.E. 2/4 (Inst.) I – Semester (Suppl.) Examination, June 2013

Subject: Network Theory

Time: 3 Hours **Max.Marks: 75**

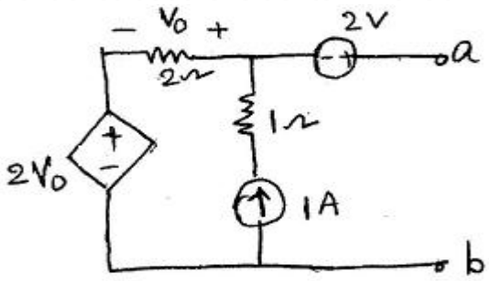
Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1. A 20 μf capacitor is connected in parallel with a 40 μf capacitor and the combination is connected across a time varying voltage source. At a particular time, the current supplied by the source is 5A obtain the magnitude of instantaneous currents through the individual capacitors. (3)
2. State and explain the superposition theorem. (2)
3. A dc constant voltage source feeds a resistance of 200 kΩ in series with a 5 μf capacitor. Find the time taken for the capacitor when the charge retained will be decayed to 50% of the initial value, the voltage source being short circuited. (3)
4. What do you understand by initial conditions? Explain. (2)
5. The current in the resistive branch of a parallel RC circuit is given by $i_r = 10\cos(1000t-10^o)$A. What is the current in the capacitance? Assume R=10 kΩ, C = 10 μf (3)
6. A series circuit has R=4Ω & L=10.01H. Find the impedance at 500Hz. (3)
7. In two wattmeter method of measuring three phase power in a balanced load, compute the p.f. of the load if reading of one wattmeter is double that of the other. (2)
8. Define bandwidth and selectivity with respect to series RLC circuit. (2)
9. Explain the Z parameters of a two port network. (2)
10. The Z parameters of a two port network are Z_{11}=10Ω, Z_{22}=20Ω, $Z_{12} = Z_{21}$ = 5Ω. Find its equivalent T-network. (3)

PART – B (50 Marks)

11. Find Norton's equivalent circuit at the left of terminal ab. (10)



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