CS 204

COMPUTER ARCHITECTURE

Course Objective:

- To introduce stored program organization of computer and instruction set architecture.
- To introduce design of control unit using microprogramming, RISC and interrupt handling.
- To introduce different microarchitectural designs such as pipelining.Vector processing and SIMD array processor.
- To introduce different algorithms used in the design of ALU
- To introduce different I/O organization mechanisms and modes of data transfer from I/O subsystem to CPU.
- To introduce various parts of a system memory hierarchy.

UNIT-I

Register Transfer and Microoperations: Register transfer language, Register Transfer, Bus and, Memory Transfers, Arithmetic Microoperations: Binary Adder, Subtractor, Binary Incrementer, Arithmetic Circuit**.** Logic Microoperations: List of Logic Microoperations, hardware Implementation. Arithmetic.Logic Shift unit.

Basic Computer Organization and Design: Instruction Codes: Stored program organization, Indirect Address. Computer Registers: Common Bus System. Computer Instructions: Instruction Set Completeness. Timing and Control, Instruction Cycle: Fetch and Decode, Register Reference Instructions. Memory Reference Instructions: Example Instructions, Control Flow Chart. Input-Output and Interrupt: Configuration, Instructions, Program Interrupt, Interrupt Cycle. Complete Computer Description. Design of Basic Computer, Basics of Accumulator Logic.

UNIT-II

Microprogrammed Control: Control Memory, Address Sequencing: Control Branching Mapping of Instruction, Subroutines. Microprogram Example: Computer Configuration, Microinstruction Format, Symbolic Microinstructions.The Fetch Routine, Symbolic Microprogram, Binary Microprogram. Design of Control Unit: Microprogram Sequencer Central Processing Unit: General Register Organization: Control World Stack Organization: Register Stack, Memory Stack, Reverse Polish Notation, Evaluation of Expressions. Instruction Formats: Three, Two, One, Zero Address Instructions, RISC Instructions. Addressing Modes.DataTransfer and Manipulation: Data Transfer Instructions, Data Manipulation Instruction, Arithmetic Instruction Logical, Shift and Bit Manipulation Instructions.

Program Control: Status Bit Conditions, Conditional Branch Instructions Subroutine Call and Return, Program Interrupt, Types of Interrupts, Reduced Instruction Set Computer: CISC.

Characteristics, RISC Characteristics, Overlapped Register Windows.

UNIT-III

Pipeline and Vector Processing: Parallel Processing, Pipelining, Instruction Pipeline, RISC Pipeline, Vector Processing: Vector Operations, Matrix Multiplication, Memory Interleaving, Super Computers. Array Processors: Attached Array Processor, SIMD Array Processor.

Computer Arithmetic: Addition and Subtraction: With Signed Magnitude Data, Implementation and algorithm, Addition and Subtraction with 2's Complement Data. Multiplication Algorithms with signed magnitude data, algorithm, Booth's algorithm, Array multiplier. Division Algorithms with signed magnitude data, divide overflow, algorithm. Floating Point Arithmetic Operations, Decimal Arithmetic Unit: BCD Adder, Subtractor.

UNIT-IV

Input Output Organization: Input-Output Interface: I/O Bus and Interface Modqles, I/O Versus Memory Bus, Isolated vs Memory Mapped I/O. Asynchronous Data Transfer: Strobe Control, Handshaking, Asynchronous Serial Transfer, Asynchronous Communication Interface.

Modes of Transfer: Programmed I/O, Interrupt driven I/O. Priority Interrupt: Daisy Chaining, Parallel Priority Interrupt, priority Encoder. Direct Memory Access**:** DMA Controller and Transfer. Input-Output Processor (lOP): CPU-IOP Communication, IBM 370 I/O Channel, Intel 8089-IOP. Serial Communication.

UNIT-V

Memory Organization: Memory Hierarchy, Main Memory**:** RAM and ROM Chips, Address Map, Memory Connection to CPU. Auxiliary Memory**:** Disks and Tapes. Associative Memory**:** Hardware Organization, Match Logic, Read. Operation and Write Operation. Cache

Memory: Associative Mapping, Direct. Mapping, Set-Associative Mapping, Writing into Cache Initialization. Virtual Memory**:** Address and Memory Space, Address Mapping, Page Replacement.

Suggested Reading:

1.M. Morris Mano, *Computer System Architecture*, 3rd edition, Pearson Education Asia, 2002.

2.William Stallings, *Computer Organization & Architecture*, 6th Edition, Pearson Education Asia, 2003.

3.V.CarlHamacher, Z.G Vranesic, S.G. Zaky, *Computer Organization,* McGraw Hill, 2004.

4.David A. Patterson, John L. Hennessy, *Computer Organization and Design.* Morgan, Elsevier Inc, 2009.