Code No. 2216

FACULTY OF INFORMATICS

B.E. 3/4 (IT) II-Semester (Supplementary) Examination, January 2013

Subject : Computer Graphics (Elective-I)

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. What is Persistence? (2)
2. Differentiate Raster scan and Random scan displays. (3)
3. What are Bundled Attributes? (2)
4. Give the transformation matrix of viewing transformation. (2)
5. Classify interactive input devices. (2)
6. What are editing structures? (3)
7. What is an octtree? (2)
8. What are Bazier curves? Give an example. (3)
9. Write the steps for Liang Bensky lien clipping. (3)
10. State parametric continuity conditions. (3)

PART – B (5x10=50 Marks)

11.(a) What are the differences between Bresenham's line drawing and DDA line drawing algorithms?
(b) Describe the Bresenham's line drawing algorithm for all quadrants.

12. Find transformation matrix that transforms the given polygon V_1, V_2, V_3, V_4 to half its size with centre still remaining at the same position $V_1(1, 1)$, $V_2(3, 1)$, $V_3(3, 3)$, V4(1, 3) and centre (2, 2). Find new coordinates of polygon.

13.(a) Describe Cohen Sutherland line clipping algorithm. Using this algorithm clip the following line segments against a window $wx_1=50$, $wy_1=50$, $wx_2=100$, $wy_2=100$
(i) line P_1P_2 $P_1(80, 30)$ $P_2(90, 60)$
(ii) line P_3P_4 $P_3(60, 60)$ $P_4(70, 70)$
(iii) line P_5P_6 $P_5(30, 70)$ $P_6(70, 120)$
(iv) line P_7P_8 $P_7(120, 60)$ $P_8(125, 80)$

14.(a) How hierarchical modeling is done with structures?
(b) Explain perspective projection operation.

15.(a) Write about B-spline curves and surfaces.
(b) Give an algorithm for visible surface detection.

16.(a) Explain all 2D Transformations and give the homogeneous transformation matrices for them.
(b) Explain CSG methods.

17. Write short notes on the following:
(a) Back face detection Algorithm
(b) Scan line Fill Algorithm
(c) Flat panel displays

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Code No. 2215

FACULTY OF INFORMATICS

B.E. 3/4 (IT) II-Semester (Supplementary) Examination, January 2013

Subject : Compiler Construction
(Elective-I)

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. List the major data structures used in a compiler. (2)
2. Write a regular expression to identify floating point numbers. (3)
3. What is Dangling-else problem? Give an example. (3)
4. What is parse tree? Give an example. (2)
5. Write the conflicts that occur during shift-reduce parsing. (3)
6. Write LR (0) items for the following grammar A → (A) / a (2)
7. Define synthesized and inherited attributes. (3)
8. What is a symbol table? What are its contents? (2)
9. Write the following expression in quadruple form
   (a + b) * (c + d) + (a + b + c) (3)
10. What is Back patching? (2)

PART – B (5x10=50 Marks)

11.(a) Construct a DFA for the following regular expression (10)
   (a + b)* (aa + bb) (a + b)*
   (b) Write algorithm for subset construction and trace above DFA.

12. Verify whether the following grammar is LL(1) or not by constructing parsing table
   $S \rightarrow I\ AB / \in$ (10)
   $A \rightarrow I\ AC / OC$
   $B \rightarrow OS$
   $C \rightarrow I$

13. Construct a DFA of LR(0) items for the following grammar. (10)
   $S \rightarrow CC$
   $C \rightarrow aC / b$

14.(a) Write about static and dynamic storage allocation strategies. (5)
   (b) Write about various parameter parsing mechanisms with suitable examples. (5)

15.(a) Write an algorithm for simple code generator. (5)
   (b) Explain code generation of control statements and logical expressions. (5)

16.(a) Discuss about loop optimization techniques. (5)
   (b) Construct a DAG for the given blocks (5)
   a : = b + c
   b : = b - d
   c : = c + d
   e : = b + c

17. Write short notes on the following: (10)
   (a) Error Recovery in Bottom – up parsers
   (b) Properties of CFLs
   (c) Bootstrapping compliers

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Code No. 2217

FACULTY OF INFORMATICS

B.E. 3/4 (IT) II-Semester (Supplementary) Examination, January 2013

Subject : Advanced Computer Architecture
(Elective-I)

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. Sketch a block diagram to represent the architecture of a vector super computer. (2)
2. Illustrate detection of parallelism in a program using Bernstein's conditions. (3)
3. List some primitive operations for vector processors and symbolic processors. (2)
4. What are the forbidden latencies and the initial collision vector for the reservation table for a four stage pipeline with a clock cycle T = 20 m shown below. (3)

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

5. Show how Butterfly network is a restricted subclass of omega networks. (3)
6. State and explain briefly any two context switching policies in multithreaded architectures. (2)
7. What is the purpose of loop parallelization? Give the two steps to perform loop parallelization. (3)
8. Describe parallel flow control. (3)
9. List parallel languages for parallel programming. (2)
10. How is asynchronous message passing achieved in Linda programming? (2)

PART – B (5x10=50 Marks)

11. (a) Illustrate the following: (5)
    (i) Data dependence (ii) control dependence (iii) resource dependence
    (b) Draw dependences graph and parallel execution flow using adders for the following instructions labeled p_1, p_2, p_3, p_4 and p_5. (5)
    p_1 : C = D X E
    p_2 : M = G + C
    p_3 : A = B + C
    p_4 : C = L + M
    p_5 : F = G ÷ E
    Assume each statement requires one step to execute.

12. (a) The performance of memory hierarchy is determined by the 'effective accesstime' at any level in the hierarchy, and depends on the 'nitrations' and 'access frequencies'. Explain. (5)
    (b) Give a Hierarchy optimization model and explain. (5)

13. (a) Explain cache coherence problem. (5)
    (b) Illustrate Snoopy Bus protocol. (5)

14. Describe in detail the share – variable model as a parallel programming model. (10)

15. (a) Explain synchronous message passing with special reference to Ada. (5)
    (b) Illustrate Domain decomposition. (5)

16. Give SIMD machine model. Write vector instruction types along with examples. (10)

17. Write short notes on the following: (10)
    (a) Conditions for parallelism
    (b) Multithreading Issues and solutions
    (c) Language features for parallelism

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